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RM-7063

B. E. III (Sem. VI) (CO) Examination

May / June – 2010

Computer Organization

Time : 3 Hours] [Total Marks : 100

Instruction :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. 3 (Sem. 6) (CO)

Name of the Subject :

☛ Computer Organization

☛ Subject Code No. : 7 0 6 3 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

SECTION - I

Q 1 A Do as directed **10**

1. Define microinstruction. 1
2. PUSH A, is an example of one address instruction. (True/False) 1
   TRUE
3. List the four major groups of computers according to Flynn's classification. (SISD,SIMD,MIMD,MISD) 1
4. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. 3
   i. How many bits are there in the operation code, the register code part, and the address part?
   ii. Draw the instruction word format and indicate the number of bits in each part.
   iii. How many bits are there in the data and address inputs of the memory? (5.14)
5. Give the difference between Subroutine call and interrupt routine. 1
6. Give full form of ISZ and BSA. 1
7. List types of interrupts. (External interrupt, internal interrupt and software interrupt) 1
8. What is meant by 'Prefetch Target Instruction' in pipeline? 1

Q.1 **B** **10**

1 A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500. 6

i. What should be the value of the relative address field of the instruction (in decimal)?

ii. Determine the relative address value in binary using 12 bits.

iii. Determine the binary value in PC after the fetch phase and calculate the binary value of 500. then show that the binary value in PC plus the relative address calculated in part (ii) is equal to binary value of 500.

2 Differentiate computer architecture and computer organization. (3) 4

Q.2 **A** Define addressing mode and explain with an example. 7

i. Relative addressing mode

ii. Indexed addressing mode.

iii. Base register addressing mode.(260-264)

OR

A Draw and explain flowchart for instruction cycle with interrupt of the basic computer. (158) 7

B Explain micro programmed control organization with block diagram. (214) 5

Q.3 **Attempt any three** 18

1. A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 30ns. Determine the speedup ratio of the pipeline for 120 tasks. What is the maximum speedup that can be achieved? (
2. Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has six bits and the control memory has 2048 words
3. Convert the following arithmetic expressions from infix to reverse polish notation.

   i. $(((A/(B*C))+(D*E))-(A*C))$

   ii. $(A+B)*(C+D-E)*F$

4. Write a program to evaluate the arithmetic expression:

$$X=(A+B)*(C+D)$$

i. Using a general register with three address instructions.

ii. Using a general register with two address instructions.

SECTION - II

Q.4 (a) Do as directed: 10

1. Define : Hit Ratio 3
   System Bus
   Baud rate
2. What is the use of valid bit in cache memory? 1
3. What is comparison method for binary division? 2
4. What is cycle stealing in DMA? 1
5. What is page fault? 1
6. What is zero insertion in bit oriented protocol? (439) 1
7. Multiprocessors are classified as _____ systems. 1

Q.4 (b)Explain with flowchart multiplication of binary integers in signed 2's complement representation. 8

Or

(b) Explain with flowchart addition and subtraction of floating point numbers. 8

Q.5 (a) What is mapping? Explain three types of mapping considering the organization of cache memory. 8

(b) What is DMA? Explain DMA transfer in a computer system. 6

Or

(a) Do following :

1. A two way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K × 32. 4
   a. formulate all pertinent information required to construct the cache memory.
   b. what is the size of the cache memory?

2. The access time of a cache memory is 100ns and that of main memory 1000ns. it is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The hit ratio for read accesses only is 0.9; a write through policy is used. 4
   A. what is the average access time of the system considering only memory read cycles?
   B. what is the average access time of the system for both read and write requests?

(b) Explain three modes of data transfer to and from peripherals. 6

(c) Explain interrupt cycle with sequence of micro operations. 2

Q.6 Answer the following. (any four) 16

1. BCD adder
2. virtual memory
3. Isolated Vs. Memory mapped I/O.
4. Explain dynamic arbitration algorithms.
5. Cache coherence